

Listing Of Claims

Claims 1-46 (Canceled)

47. (previously presented) A semiconductor component comprising:

a semiconductor die having a face and a plurality of die contacts on the face in a pattern;

an electrically insulating layer on the face;

a plurality of redistribution conductors on the layer in electrical communication with the die contacts configured to redistribute the pattern of the die contacts;

an electrically insulating outer layer on the conductors and the layer having a plurality of openings aligned with selected portions of the conductors configured in an area array; and

a plurality of bumped contacts in the openings bonded to the selected portions of the conductors.

48. (previously presented) The component of claim 47 wherein the bumped contacts comprise solder balls and the area array comprises a grid array.

49. (previously presented) The component of claim 47 further comprising a plurality of under bump metallization layers on the selected portions configured to facilitate bonding of the bumped contacts to the redistribution conductors.

50. (previously presented) The component of claim 47 wherein the die is contained on a semiconductor wafer.

51. (previously presented) The component of claim 47 wherein the die has a plurality of edges and the redistribution conductors fan out the pattern of the die contacts to the edges.

52. (previously presented) The component of claim 47 wherein the die has a plurality of edges and the redistribution conductors fan in the pattern of the die contacts from the edges.

53. (previously presented) A semiconductor component comprising:

- a semiconductor die comprising a face and a plurality of die contacts on the face in a pattern;

- an electrically insulating layer on the face;

- a plurality of conductors on the electrically insulating layer in electrical communication with the die contacts configured to redistribute the pattern of the die contacts;

- a dielectric layer on the conductors and the electrically insulating layer having a plurality of openings in an area array aligned with selected portions of the conductors;

- a plurality of under bump metallization layers on the selected portions; and

- a plurality of bumped contacts on the under bump metallization layers.

54. (previously presented) The component of claim 53 further comprising a plurality of second openings in the dielectric layer and a plurality of test contacts in the

second openings aligned with other portions of the conductors.

55. (previously presented) The component of claim 53 wherein the area array comprises a grid array.

56. (previously presented) The component of claim 53 wherein the die has a plurality of edges and the conductors fan out the pattern of the die contacts to the edges.

57. (previously presented) The component of claim 53 wherein the die has a plurality of edges and the conductors fan in the pattern of the die contacts from the edges.

58. (previously presented) The component of claim 53 wherein the dielectric layer comprises a material selected from the group consisting of polyimide, glasses, and oxides.

59. (previously presented) The component of claim 53 wherein the dielectric layer comprises a photoimageable material.

60. (previously presented) A semiconductor component comprising:

- a semiconductor die comprising an electrically insulating die passivation layer and a plurality of die contacts;

- a plurality of redistribution conductors on the die passivation layer in electrical communication with the die contacts having selected portions arranged in an area array;

a plurality of terminal contacts on the selected portions; and

an electrically insulating outer passivation layer on the conductors and the die passivation layer having a plurality of openings for the terminal contacts aligned with the selected portions.

61. (previously presented) The component of claim 60 further comprising a plurality of test contacts comprising second portions of the conductors and second openings in the outer passivation layer.

62. (previously presented) The component of claim 60 wherein the area array comprises a grid array.

63. (previously presented) The component of claim 60 wherein the terminal contacts comprise under bump metallization layers and solder bumps on under bump metallization layers.

64. (previously presented) The component of claim 60 wherein the die is contained on a semiconductor wafer containing a plurality of dice substantially similar to the die.

65. (previously presented) The component of claim 60 wherein the die has a plurality of edges and the conductors fan out the pattern of the die contacts to the edges.

66. (previously presented) The component of claim 60 wherein the die has a plurality of edges and the conductors fan in the pattern of the die contacts from the edges.

67. (previously presented) The component of claim 60 wherein the die contacts comprise bond pads.